WHAT IS CLAIMED IS:

1. A control unit of an input/output node for a computer system comprising:

a plurality of scheduler units including:

a first buffer circuit coupled to receive control commands from a first source, wherein said first buffer circuit includes a first plurality of buffers each corresponding to a respective virtual channel of a plurality of virtual channels for storing selected control commands that belong to said respective virtual channel;

a second buffer circuit coupled to receive control commands from a second source, wherein said second buffer circuit includes a second plurality of buffers each corresponding to a respective virtual channel of said plurality of virtual channels for storing selected control commands that belong to said respective virtual channel; and

an arbitration unit coupled to said first buffer circuit and to said second buffer circuit, said arbitration unit is configured to arbitrate between said control commands stored in said first buffer circuit and said control commands stored in said second buffer circuit.

2. The control unit as recited in claim 1, wherein said arbitration unit is configured to arbitrate based upon a set of predetermined criteria.

3. The control unit as recited in claim 2, wherein said set of predetermined criteria includes an arbitration algorithm and a determination of whether storage space is available within a destination buffer.

4. The control unit as recited in claim 1, wherein said arbitration unit is further configured to provide an indication to said first source in response to selecting said control commands stored in said first buffer circuit during arbitration.

5. The control unit as recited in claim 4, wherein said arbitration unit is further configured to provide an indication to said second source in response to selecting said control commands stored in said second buffer circuit during arbitration.

6. The control unit as recited in claim 1, wherein said plurality of virtual channels includes a posted channel, a non-posted channel and a response channel.

7. The control unit as recited in claim 1, wherein each of said first plurality of buffers and each of said second plurality of buffers are FIFO buffer structures including a plurality of storage locations.

8. An input/output node for a computer system comprising:

a first source unit;

a second source unit; and

a control unit coupled to said first unit and said second source unit, said control unit includes a plurality of scheduler units each including:

a first buffer circuit coupled to receive control commands from said first source unit, wherein said first buffer circuit includes a first plurality of buffers each corresponding to a respective virtual channel of a plurality of virtual channels for storing selected control commands that belong to said respective virtual channel;

a second buffer circuit coupled to receive control commands from said second source unit, wherein said second buffer circuit includes a second plurality of buffers each corresponding to a respective virtual channel of said plurality of virtual channels for storing selected control commands that belong to said respective virtual channel; and

an arbitration unit coupled to said first buffer circuit and to said second buffer circuit, said arbitration unit is configured to arbitrate between said control commands stored in said first buffer circuit and said control commands stored in said second buffer circuit.

9. The input/output node as recited in claim 8, wherein said arbitration unit is configured to arbitrate based upon a set of predetermined criteria.

10. The input/output node as recited in claim 9, wherein said set of predetermined criteria includes an arbitration algorithm and a determination of whether storage space is available within a destination buffer.

11. The input/output node as recited in claim 8, wherein said arbitration unit is further configured to provide an indication to said first source unit in response to selecting said control commands stored in said first buffer circuit during arbitration.

12. The input/output node as recited in claim 11, wherein said arbitration unit is further configured to provide an indication to said second source unit in response to selecting said control commands stored in said second buffer circuit during arbitration.

13. The input/output node as recited in claim 8, wherein said plurality of virtual channels includes a posted channel, a non-posted channel and a response channel.

14. The input/output node as recited in claim 8, wherein each of said first plurality of buffers and each of said second plurality of buffers are FIFO buffer structures including a plurality of storage locations.